REMARKS

Claims 1-31 were pending at the time of this Office Action. Claim 2 has been amended. No other claims have been amended. Thus, claims 1-31 are present for examination. Reexamination and reconsideration of the application, in view of the following remarks, are requested.

Claims 1-3, 5-7, 15, and 22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wu, U.S. Patent Number 5,774,551.

The rejection is respectfully traversed for at least the following reasons.

Independent claim 1 recites, among other features, a control unit having a data input bus, at least one encryption processing unit, first and second authentication processing units, a local data bus (that is independent of the data input bus), and a second data bus connecting the encryption processing unit to each authentication processing unit.

Wu does not disclose each of the features recited in claim 1. For example, Wu discloses only a single processing unit – the CPU 115. [Wu, Figure 115.] Claim 1, on the other hand, recites at least four processing units – the control unit, the at least one encryption processing unit, and the first and second authentication processing units. The examiner suggests that Wu discloses an encryption processing unit at col. 3, lns. 58-62. However, a thorough review of that section reveals that the encryption process is actually a part of Wu's authentication services. [Wu, col. 3, lns. 55-66.] Also, the examiner suggests that Wu discloses first and second authentication processing units at col. 8, lns. 61-66. However, this section also refers to the authentication services 109. Wu's authentication services 109 are not authentication processing units at all; but rather they are computer programs

stored in an addressable memory 103. [Wu, col. 5, lns. 7-10.] Wu discloses that the authentication services 109 are stored in a computer 101 that has a single processor 115. [Wu, col. 4, lns. 63 through col. 5, lns. 6.] Thus, in Wu, each of the authentication services 109, along with any encryption service, is necessarily processed by Wu's single processor 115. Because Wu employs a single processor 115, Wu does not disclose the multiple processing units recited in claim 1.

In addition, claim 1 recites a second data bus from the encryption processing unit to the authentication processing unit. This second data bus is neither disclosed nor suggested in Wu. The examiner suggests that Wu's pluggable account management interface 123 is a second data bus. However, Wu's account management interface 123 is not a bus at all, but rather it is a "library of software methods" that the system invokes to obtain functionality from certain services. [Wu, col. 6, lns. 16-28.] Moreover, as discussed above, because Wu does not disclose separate encryption processing units and authentication processing units, Wu could not disclose a data bus connecting those units. Wu's "processing units" are actually programs stored in a common memory 129 that are executed by the single processor 115. Thus, Wu could not and does not disclose or suggest the second data bus recited by claim 1.

Because claim 1 recites features that are neither disclosed nor suggested in the the prior art of record, the rejection of claim 1 under 35 U.S.C. § 102 is respectfully traversed. Claims 2-4 are all dependent on claim 1. Thus, the rejection of claims 2-4 is likewise traversed.

Moreover, claim 2 recites a data input bus coupled to a processor bus. Wu does not disclose a data input bus coupled to a processor bus. Indeed, as discussed above, Wu does not disclose a processor bus. Claim 2 further recites

that the data input bus and the processor bus are also coupled to each of the encryption and authentication processing units. The examiner suggests, at page 7 of the Office Action, that it is inherent that the services are connected to each other by means of hardwire lines in order to communicate with each other. [Office Action, p. 7.] However, the services to which the examiner refers are actually computer programs. Thus, there could be no hardwire lines or bus connecting them. Accordingly, the rejection of claim 2 is respectfully traversed.

Claim 3 recites that the data input bus is coupled to a processor bus; and that each of the processing units comprises a data input bus to the processor bus. For at least the reasons discussed above, Wu does not disclose each of the features recited in claim 3. For example, as discussed above, Wu does not disclose a data input bus coupled to a processor bus. Thus, the rejection of claim 3 is respectfully traversed.

Claim 5 recites features that are neither disclosed nor suggested in Wu. For example, claim 5 recites a plurality of processing units that are in data communication with the control unit. As discussed above, Wu does not disclose a plurality of processing units. Rather, Wu discloses a single processing unit 115. Also, claim 5 recites a second data bus that is independent of the first data bus. As discussed above, Wu does not disclose a second data bus. Further, claim 5 recites processing data of first and second data packets in the multiple processing units. Claim 5 further recites communicating output data from a first processing unit to a second processing unit when the first processing unit completes its processing so that the first processing unit can process another data packet. These features are neither disclosed nor suggested in Wu. Thus, for at least these reasons, the rejection of claim 5 is respectfully traversed.

Claims 4 and 8-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu.

The rejection of claims 4 and 8-31 is respectfully traversed for at least the following reasons.

Claim 4 recites features that are neither disclosed nor suggested in the prior art of record. For example, claim 4 recites that the second data bus comprises a daisy-chain connection between the multiple processing units. As discussed above, Wu does not disclose multiple processing units. Further, the examiner correctly notes that Wu does not disclose a second data bus comprising a daisy-chain connection between the encryption and authentication processing units. The examiner, however, takes Official Notice that the chain is well known in the art because it is widely used to eliminate conflicting requests to use the bus. [Office Action, p. 3.] Applicant submits that the features recited in claim 4 are neither obvious nor well known in the art. Applicant employs the daisy-chain bus connection so that the packet processor may process multiple packets simultaneously. Processing of a second packet can begin as soon as resources become available, even if the processing of a first packet has not been completed. In addition, by coupling the encryption unit 108 and the authentication units 110 and 112 to the daisy-chain bus, rather than to the processor bus 102, traffic on the processor bus 102 is minimized. Thus, applicant believes that the daisy-chain connection recited in claim 4 is not obvious.

If the examiner still considers the daisy-chain bus connection to be "well known," then the applicant respectfully requests that the examiner cite a reference or references disclosing these features. [MPEP § 2144.03.] The applicant would like to have an opportunity to address any particular prior art

reference that the examiner believes discloses or suggests the daisy-chain bus connection recited in claim 4.

Independent claims 9, 10, 15, 16, 17, 22, 23, 24, 29, and 30 recite various methods, apparatus', and articles of manufacture comprising performing encryption on a first data packet within an encryption processing unit or module. After completion of the encryption, authentication of the first data packet is performed by at least one authentication unit or module. Encryption is performed on a second data packet prior to completion of the authentication of the first data packet.

The features recited in claims 9, 10, 15, 16, 17, 22, 23, 24, 29, and 30 are neither disclosed nor suggested in the prior art of record. For example, as discussed above, Wu does not disclose multiple processing units or modules. Thus, the rejection is traversed for at least the reasons discussed above. Moreover, the examiner correctly notes that Wu also does not disclose performing encryption on a first data packet and, after completion of the encryption of the first data packet, performing authentication of the first data packet while performing encryption of a second data packet. However, the examiner takes Official Notice that these features are well known in the art. [Office Action, p. 4.] The examiner discusses an example of a parallel encryption scheme where first and second packets are encrypted at the same time. [Office Action, p. 4.]

Applicant submits that the features recited in these claims are neither obvious nor well known in the art. Applicant does not disclose a parallel scheme with redundant processors. Instead, applicant discloses that by employing a multiple-processor configuration with a data bus, as soon as a single encryption processor completes encryption processing of a first packet, it

can begin encryption processing of a second packet, while the first packet is being processed by an authentication processor. Thus, multiple packets may be processed simultaneously. However, unlike a parallel processing scheme, applicant discloses employing a single encryption processor that processes all packets. This approach improves the speed at which packets are processed and it improves the utilization of the encryption processor and the authentication processors.

If the examiner still considers features of these claims to be "well known," then the applicant respectfully requests that the examiner provide a reference or references disclosing or suggesting employing multiple processors to process two data packets simultaneously, such that one packet is being encrypted by one processor while another packet, which has already been encrypted by the one processor, is being authenticated by another processor. [MPEP § 2144.03.] The applicant would like to have an opportunity to address any particular prior art reference that the examiner believes discloses or suggests features recited in these claims. Thus, the applicant respectfully traverses the rejection of claims 9, 10, 15, 16, 17, 22, 23, 24, 29, and 30.

Claims 11-14 are dependent, either directly or indirectly, on claim 10. Thus, the rejection of claims 11-14 likewise is traversed at least for the reasons discussed above. In addition, claim 11 recites performing first and second authentications on a data packet. Claim 12 recites that the first authentication is performed on a packet that has already been encrypted. Claim 13 discloses that the first authentication processor appends data to an encrypted first packet, and claim 14 recites that the second authentication processor performs authentication on the encrypted first packet and the appended data. Features recited in claims 11-14 are neither disclosed nor suggested in Wu. Thus, claims 11-14 are believed to be further distinguished from Wu.

Claims 18-21 are dependent, either directly or indirectly, on claim 17. Thus, the rejection of claims 18-21 likewise is traversed at least for the reasons discussed above. In addition, claims 18-21 are believed to be further distinguished from Wu for at least the reasons discussed above in connection with claims 11-14.

Claims 25-28 are dependent, either directly or indirectly, on claim 24. Thus, the rejection of claims 25-28 likewise is traversed at least for the reasons discussed above. In addition, claims 25-28 are believed to be further distinguished from Wu for at least the reasons discussed above in connection with claims 11-14.

Claims 31 and 32 are dependent, either directly or indirectly, on claim 30. Thus, the rejection of claims 31 and 32 likewise is traversed for at least the above reasons.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application and allowance of the claims at an early date is respectfully requested.

If, for any reason, the examiner finds the application to be in other than condition for allowance, applicant requests that the examiner contact the undersigned attorney at (310) 975-7963 to discuss any steps necessary to place the application in condition for allowance.

Respectfully submitted,

July 5, 2002
Date

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HUYNH, ET AL.

Group Art Unit: 2131

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MARKED UP COPY OF AMENDMENT AND REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Commissioner:

In reply to the Office Action mailed April 9, 2002, please amend the above-identified application as follows:

IN THE CLAIMS

Claim 2 is amended as follows:

2. (Amended) A packet processor as recited in claim 1, wherein said data input bus of the control unit is coupled to a processor bus, and

wherein each of said encryption and authentication processing units comprises a data input bus coupled to the processor bus.